Amendments to the Specification:

Please replace paragraph **[0089]** beginning on page 16 of the specification with the following amended paragraph:

[0089] **FIG. 25** illustrates a multichip module which has been manufactured by process similar to that described in a U.S. patent application Serial No. 09/904,306 entitled "Interconnect Circuitry, Multichip Module, And Methods For ~~Making Them~~ Manufacturing Thereof" filed July 12, 2001, by Peter R. Nuytkens, Ilya E. Popeko, and Joseph M. Kulinets, and now U.S. Patent No. 6,838,750 B2 issued January 4, 2005 (hereafter referred to as the ~~'306 application~~ '750 patent.) The ~~'306 application~~ '750 patent is hereby incorporated herein by reference in its entirety. It should also be noted that the '750 patent is the parent for U.S. Divisional Application Serial No. 11/010,790 filed December 13, 2004 (the '790 application).

now US PAT. D,179,742

Please replace paragraph [0104] beginning on page 18 of the specification with the following amended paragraph:

[0104] Aspects of the present invention make it possible to form ferromagnetic cores on a broad range of dielectric materials, including many smooth dielectric materials on which it has previously been difficult to perform such electroless plating. This includes, to name just a few, FR4, polyimide, BT, Teflon, and latex. The electroless plating method using the catalytic particles discussed with regard **FIG. 10** can also be used to electrolessly plate conductive layers or seed layers for electroplating of conductive layers, such as copper conductive layers, for use in the winding layers of the inductors formed by the present invention. The formation of conducting layers using such techniques is described in greater detail in the ~~'306 application~~ '750 patent referenced above.